MONOLITHIC HIGH-VOLTAGE FET POWER AMPLIFIERS*

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ABSTRACT

High-voltage field-effect transistor (HVFET) power amplifiers offer improved system efficiency through reduced DC power distribution loss and more efficient DC power conditioning. Results are presented for the first such monolithic microwave integrated circuit (MMIC) amplifiers and four-cell amplifiers at X-band. Drain bias voltages up to 40 V with such amplifiers have been achieved.

INTRODUCTION

Present field-effect transistor (FET) power amplifiers for satellite applications require a DC to DC voltage converter to transform the satellite bus voltage of 28 to 40 V to a much lower drain bias voltage (typically 8 to 10 V), as limited by the onset of avalanche breakdown in semiconductor junctions. Since the voltage converter efficiency is typically 80 percent, roughly 20 percent of the spacecraft prime power is wasted.

Figure 1 shows the potential prime power saved when FET amplifiers with higher bias voltages are used. Assuming a spacecraft with 24 8.5-W transponders and amplifiers with 30-percent power-added efficiency, DC power of 170 W may be saved for a regulated satellite bus. Future trends in satellite power systems are likely to lead to such regulated buses at voltages up to 50 or even 120 V [1]. Other advantages, such as reduced payload mass and part count, are obtained by eliminating the DC to DC voltage converter.

In phased-array applications with a large number of active devices, the I^2R power loss in the DC distribution network is quite high. Increasing the DC power supply voltage from 8 to 32 V, for example, will reduce the DC distribution loss by a factor of 16. For a phased-array system consisting of a thousand 10-W elements with a distribution cable having a resistance of only 0.001 Ω, power distribution losses will drop from more than 15 percent to less than 1 percent of the supplied DC power.

One approach to achieving high bias voltage involves connecting the DC bias of a number of FETs in series (drain to source), while combining the RF power of each FET in parallel to achieve high output power. Figure 2 shows the high-voltage FET (HVFET) topology for four cells. A two-cell microwave integrated circuit (MIC) amplifier using this concept has previously been reported [2].

The HVFET approach, although leading to high-voltage capability, presents technical challenges in two major areas. First, because the FET sources are RF-grounded through capacitors, a large capacitive reactance is presented to the FET source below the frequency of operation, and at very low frequencies appears electrically open. The stability of the amplifier must be carefully examined to prevent oscillation. Second, because the FETs are DC biased in series, any variation in the FET characteristics will produce an imbalance in DC voltage distribution, resulting in premature gate drain breakdown, inefficient RF power combining, or both. Because MMICs enjoy good uniformity in electrical characteristics of adjacent FETs, they are highly suitable for the high-voltage configuration approach. This paper presents HVFET designs and measured microwave results for two MMIC amplifiers realized using the HVFET approach. This is the first time that such MMICs have been demonstrated and that as many as four FET cells have been used.

DEVICE AND CIRCUIT DESIGN

Each cell of the HVFET consists of a FET with its source connected to a metal-insulator-metal (MIM) capacitor, the top plate of which is connected to the drain bias of the next cell through an inductor. The FETs were designed using an in-house device and circuit modeling program [3] to produce an equivalent circuit and to predict the output power and optimum load. Device structure, geometry, and material parameters were optimized for the high-voltage implementation.

Nominal gate length was 0.5 μm. Gate widths of 650 and 1,300 μm were used in the four- and two-cell implementations, respectively. The total gate width of the high-voltage amplifier was the same as that of a low-voltage amplifier of comparable output power. However, because the gate width was divided into smaller units, several advantages were realized. Large devices normally used to achieve higher power are difficult to match because of their relatively low impedances,

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and higher matching circuit loss is required. The smaller FET cells can be more efficiently matched for a given bandwidth, and, because total gate width is the same, device process yields are expected to be the same. Furthermore, because heat dissipation is distributed across several HVFET cells, lower channel temperatures and improved reliability are also expected.

Each HVFET cell has input and output impedance comparable to those of a conventional metal-semiconductor FETs (MESFET) at the frequency of operation, and the matching circuit may be designed accordingly. Input- and output-matching networks for the HVFET amplifier were optimized for gain and power over the 10.7- to 12.2-GHz satellite downlink bands. The source capacitor was chosen to be large enough to provide a good electrical short at and slightly below the frequency of operation, and small enough to avoid using unnecessary GaAs real estate. Capacitance of 30 pF was used with the FET cell of 1,300-μm gate width and 15 pF with the 650-μm cell. An R-C circuit in the gate bias network provides bias voltage through a mesa resistor and ensures stable operation below the frequency of operation. At very low frequencies, this resistor will not be terminated, as gate bias is applied through an off-chip ribbon-bond inductance. At such low frequencies the source capacitor acts like an open circuit and the FET source "sees" the output resistance of the next FET cell, which provides negative feedback and stability down to DC.

The amplifiers were fabricated using a COMSAT power MMIC process [4] on vapor phase epitaxially grown GaAs. Optical photolithography and direct electron-beam written gates were used, and via hole technology provided low-inductance grounding for the bypass capacitors. MIM capacitors consisted of 2,500-Å Si_3N_4 dielectric deposited through a plasma-enhanced chemical vapor deposition (PECVD) process. The resistors were fabricated from n+/n mesa-etched layers. Figure 3 shows a picture of the two-cell amplifier chip; die size was 2.3 x 1.9 mm. Figure 4 shows the four-cell HVFET MMIC amplifier chip; die size was twice that of the two-cell HVFET.

To achieve the appropriate biases for the individual cells, a resistive voltage divider was designed to provide the gate voltages that were positive. Comparing the amplifier performance, it was shown that there was no difference in measured gain, power, or efficiency when the resistive bias or power supplies were used. DC power consumed by the present resistive bias network was less than 2 percent of the power supplied to the amplifier.

MEASURED RESULTS

Figure 5 shows an assembled two-cell GaAs MMIC amplifier, including external divider/combiner networks fabricated on fused silica substrates. This configuration provides lower RF loss and does not require expensive GaAs real estate. Two couplers tested back-to-back achieved 0.42-dB in-band total insertion loss with maximum return loss of 14 dB at 13 GHz. Carrier length from input to output is 0.256 in. The small-signal gain response of the two-cell HVFET power amplifier at a 15-V drain bias is shown in Figure 6. Figure 7 shows the output power and power-added efficiency of this amplifier. Output power of 29 dBm with power-added efficiency of 24 percent was achieved.

Figure 8 shows the four-cell HVFET MMIC amplifier with four-way external divider/combiner networks. Insertion loss of 0.58 dB and bandwidth of 10 to 14 GHz with 20-dB return loss were achieved from two couplers measured back-to-back. Figure 9 shows measured small-signal gain performance of the amplifier. Drain bias for this measurement was 40 V, a voltage high enough for the amplifier to be biased directly at the satellite bus voltage. FET source voltages were expected to be 0, 1/4, 1/2, and 3/4 the drain voltage. Gate biases were adjusted to be 1.3 V below each of these. The voltage between the middle two FET cells was measured to be within 1 percent of half the drain voltage, indicating proper voltage distribution among the four cells. Thus, the reliability of monolithic high-voltage amplifiers should not be affected because there is no unusually high voltage stress on the FETs; the individual FET cells experienced the same voltages as conventional amplifiers. Only the passive capacitors had to endure the increased voltage, which was within the normal breakdown limit of MIM capacitors. [Independently, an experiment to measure the time-dependent dielectric breakdown (TDDB) for monolithic capacitors is underway [5].] Figure 10 shows the power and power-added efficiency of this amplifier. Best power-added efficiency was obtained at a drain voltage of 24 V, or 6 V per cell. Output power of 29 dBm and power-added efficiency of 20 percent were achieved.

Both the two-cell and four-cell amplifiers exhibited unconditional stability, with no observed spurious responses. All measured results presented were obtained from the original design with no circuit tuning. Good agreement between the predicted results and measured results has been achieved.

CONCLUSION

Successful operation of X-band monolithic high-voltage amplifiers biased directly at satellite bus voltages has been demonstrated for the first time. This will lead to improved DC-to-RF conversion efficiency in satellite transponders by allowing the elimination of an electronic power conditioner, or its replacement by a simple voltage regulator. The techniques developed are also suitable for other applications having limited prime power budgets such as active phased-array transmitters.

ACKNOWLEDGMENT

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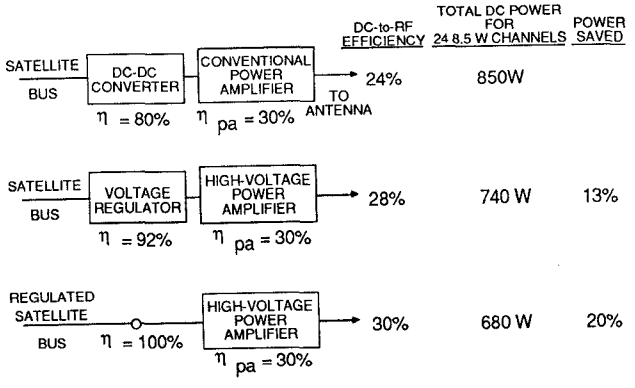

Figure 1. Comparison of Power Requirements in Conventional and High-Voltage Systems for Satellite Applications

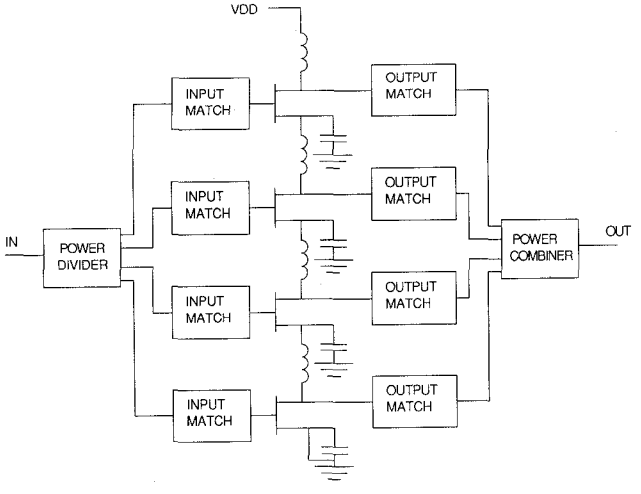

Figure 2. HVFET Amplifier Topology

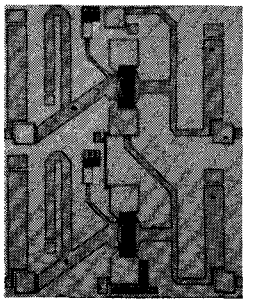

Figure 3. Two-Cell HVFET MMIC

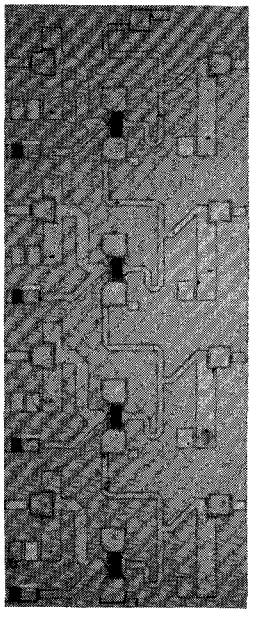

Figure 4. Four-Cell HVFET MMIC

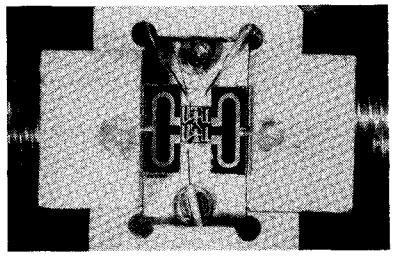

Figure 5. Two-Cell HVFET Amplifier

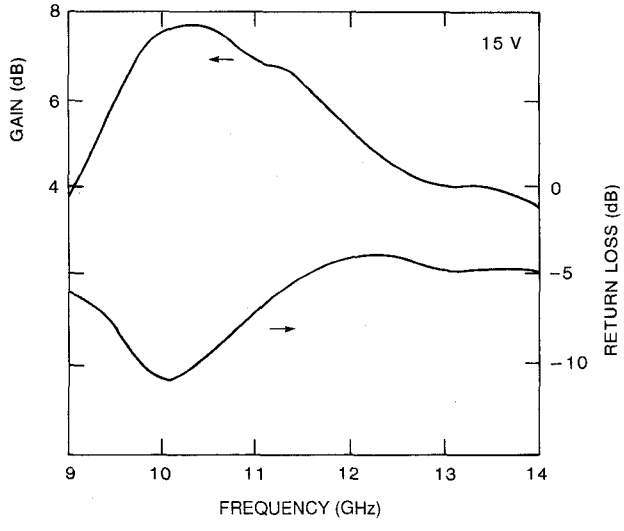

Figure 6. Frequency Response of Two-Cell HVFET Amplifier

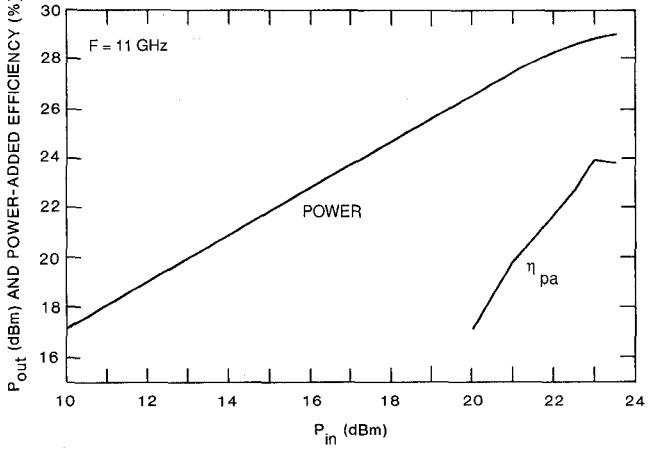

Figure 7. Power and Power-added Efficiency of Two-Cell HVFET Amplifier

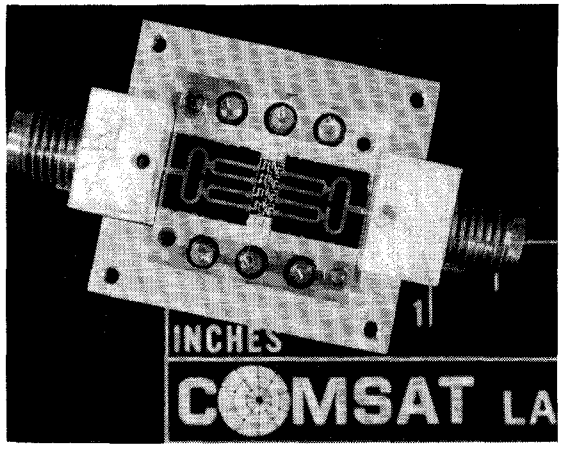

Figure 8. Four-Cell HVFET Amplifier

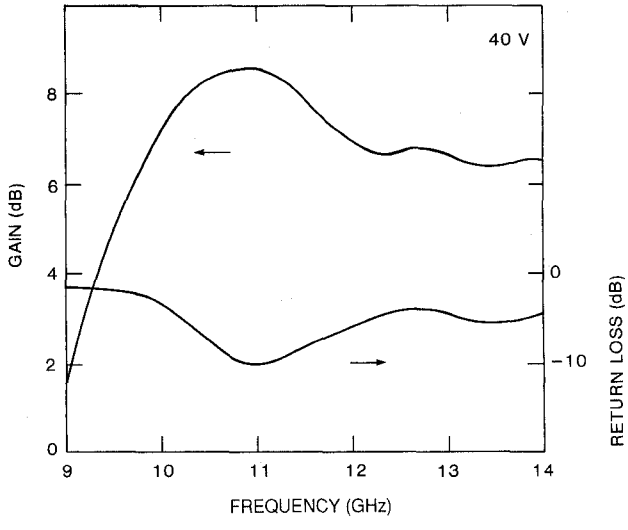

Figure 9. Frequency Response of Four-Cell HVFET Amplifier

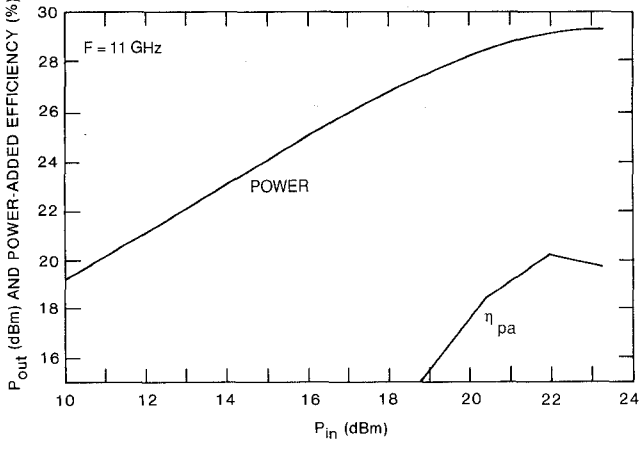

Figure 10. Power and Power-added Efficiency of Four-Cell HVFET Amplifier